

## REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-18 and 31-60 were pending. Claims 1-18 and 31-60 were rejected. In this response, no claim has been canceled. Claims 1, 4, and 7 have been amended. No new matter has been added.

Claims 1-10, 14-15, and 31-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,629,179 by Bashford (hereinafter, "Bashford") in view of U.S. Patent Number 5,956,516 by Pawlowski (hereinafter "Pawlowski"). Claims 11-13 and 16-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bashford in view of Pawlowski and further in view of U.S. Patent Number 6,564,276 by Tyner (hereinafter "Tyner").

Claims 1-18 and 31-60 include limitations that are not disclosed by the cited references, individually or in combination. Specifically, independent claim 1 as amended recites as follows:

1. A method comprising:  
receiving an interrupt from an IO device;  
converting said interrupt into an upstream memory write interrupt by generating a memory write request to a predetermined address of a memory space, the memory write request being processed via one or more memory cycles; and  
converting said upstream memory write interrupt into a front side bus (FSB) interrupt transaction, wherein one or more processors coupled to the FSB are capable of receiving the FSB interrupt as a part of a FSB transaction.

(Emphasis added)

Independent claim 1 includes converting an interrupt received from an IO device to an upstream memory write interrupt by generating a memory write request to a predetermined address of a memory space, where the memory write request being processed via one or more memory cycles. Thereafter, the upstream memory write interrupt is converted onto a front side bus (e.g., a host bus) and one or more processors coupled to the FSB may receive the FSB interrupt as a part of FSB transaction. It is respectfully submitted that the above limitations are absent from the cited references.

Rather, Bashford discloses an ordinary interrupt processing of a PCI-to-PCI bridge using an ordinary interrupt register (e.g., interrupt register 208). See, for example, Fig. 2, col. 5, lines 30-45

and Fig. 5, col. 7, lines 25-40 of Bashford. There is no mention of converting an IO interrupt to an upstream memory write interrupt, particularly, by generating a memory write request to a predetermined address of a memory space, and converting the upstream memory write interrupt into a FSB interrupt.

Pawlowski relates to a host bridge that converting interrupt request signals to interrupt message signals. Although Pawlowski discloses directing an interrupt to a host bus, Pawlowski fails to disclose converting an upstream memory write interrupt into a host bus interrupt. Specifically, Pawlowski states:

An interrupt request signal on interrupt lines 40 is provided through ports 38 and conductors 120 to I/O redirection table 128 or other processing circuitry. In response thereto, interrupt controller 34, including I/O redirection table 128, provides an interrupt message to a processor. The interrupt message may be provided through serial bus 28 through serial bus controller 144 or through processor bus 26 through encode/decode logic 148. In the case of sending the interrupt message over processor bus 26, processor 12 would include decode circuitry to detect the interrupt message and interrupt controller 24 would understand the message.

In response to receiving an interrupt request signal, at least a portion of which is in the form of address signals, interrupt controller 34 provides an interrupt message to serial bus 28 or processor bus 26. In one embodiment, host bridge 16 can direct the interrupt message either through serial bus 28 or processor bus 26 depending on a bit in control logic 130.

(Pawlowski, Fig. 2, col. 4, lines 22 to 41)

It is respectfully submitted that there is no mention of converting an upstream memory write interrupt into a FSB interrupt in Pawlowski. It is respectfully submitted that Bashford and Pawlowski, individually or in combination, fail to disclose or suggest using an upstream memory write interrupt to direct an IO interrupt to a host bus interrupt. Tyner also fails to disclose the limitations set forth above.

In addition, there is no suggestion within the cited references to combine with each other. Even if they were combined, such a combination would still lack the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claims 4, 7, 10, 31, 34, 37, 44, 51, and 59 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claims 4, 7, 10, 31, 34, 37, 44, 51, and 59 are patentable over the cited references.


Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,  
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 6/15/2004

  
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